



LAWRENCE
LIVERMORE
NATIONAL
LABORATORY

Micro-fabrication Techniques for Target Components

R. Miles, J. Hamilton, J. Crawford, S. Ratti, J. Trevino,
T. Graff, C. Stockton, C. Harvey

June 19, 2008

Fusion Science and Technology

Disclaimer

This document was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor Lawrence Livermore National Security, LLC, nor any of their employees makes any warranty, expressed or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or Lawrence Livermore National Security, LLC. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or Lawrence Livermore National Security, LLC, and shall not be used for advertising or product endorsement purposes.

Micro-fabrication Techniques for Target Components

Robin Miles, Julie Hamilton, Jackie Crawford, Susan Ratti, Jim Trevino, Tim Graff, Cheryl Stockton, Chris Harvey

Micro-fabrication techniques, derived from the semi-conductor industry, can be used to make a variety of useful mechanical components for targets. A selection of these components including supporting cooling arms for prototype cryogenic inertial confinement fusion targets, stepped and graded density targets for materials dynamics experiments are described. Micro-fabrication enables cost-effective, simultaneous fabrication of multiple high-precision components with complex geometries.

Micro-fabrication techniques such as thin-film deposition, photo-lithographic patterning and etch processes normally used in the semi-conductor manufacture industry, can be exploited to make useful mechanical target components. Micro-fabrication processes have in recent years been used to create a number of micro-electro-mechanical systems (MEMS) components such as pressure sensors, accelerometers, ink jet printer heads, microfluidics platforms and the like. [1,2] These techniques consist primarily of deposition of thin films of material, photo-lithographic patterning and etching processes performed sequentially to produce three dimensional structures using essentially planar processes. While the planar technology can be limiting in terms of the possible geometries of the final product, advantages of using these techniques include the ability to make multiple complex structures simultaneously and cost-effectively. Target components fabricated using these techniques include the supporting cooling arms for cryogenic prototype fusion ignition targets, stepped targets for equation-of-state experiments, and graded density reservoirs for material strength experiments.

Silicon support cooling arms prototype inertial fusion confinement (ICF) targets for targets

One of the prime objectives of the National Ignition Facility (NIF) is to further the state-of-the-art of laser-driven inertial confinement fusion technology. Targets built as part of the NIF ignition campaign to induce a fusion reaction within a target capsule are supported within the target chamber at the ends of long arms which hold the target in position at the center of the target chamber. The support arms terminate at an aluminum can, part of the thermal mechanical package, which holds the target hohlraum. The final ends of the support arms must grip the hohlraum can in a precise configuration to maintain the temperature of the hohlraum at 18.3° K temperature. Temperature differences across the target must be less than 0.5° mK. This can be achieved by using an intricate design at the joint between the support arm and the hohlraum can which guides the heat path symmetrically in a ring around the joint. Silicon etching techniques can be used to create these complex heat paths. Silicon also has the advantage of relatively good thermal conductivity properties ($149 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$ (at 300° K)) better than platinum ($71.6 \text{ W}\cdot\text{m}^{-1}\cdot\text{K}^{-1}$ (at 300° K)), the material of choice for previous designs and at a significantly lower cost. The integral silicon spring flexures at the ring joint of the arms grip the hohlraum can and flex to compensate for dimensional changes resulting from cooling the

target from room temperature to cryogenic conditions. Fabrication of the complex features shown in Figure 1 are performed cost-effectively at the wafer level, 8 to 10 arms per wafer, using one etch through a nominal 525 μm thick wafer. Metal traces along the length of the arms, similar to those seen on printed circuit boards, provide the electrical wiring for temperature sensors and temperature adjustment heaters located on both the arms and the hohlraum. Wire leads are fed through holes in the base of the arm and glued using conductive epoxy to the metal traces shown in Figure 2. The metal traces terminate at the thermal sensor and resistive heater mounted directly to the arm to both measure and adjust the arm temperature. Additional metal traces are used to attach to a thermal sensor and resistive heater mounted to the can of the hohlraum.

The process for making the arms is shown schematically in Figure 3. A silicon wafer roughly 525 μm thick and 100 mm in diameter is initially coated with a thin 100 nm thick, insulating silicon dioxide layer followed by a 10 nm thick chromium adhesion layer under a 1 μm thick layer of gold. The metal traces are photolithographically defined through a process of patterning and selectively etching the metal according to the pattern. The first step of this process is to spin photo-sensitive resist over the metalized wafer. A photomask, a glass plate upon which a thin chromium layer is patterned to resemble the desired metal traces, is inserted into an EV Group aligner between the silicon wafer and a UV light source. The UV light source exposes the photo-resist in areas not shadowed by the chromium on the photomask. When developed, the photo-sensitive resist is removed in the exposed areas. The gold and chromium layers on the silicon wafer are removed from these areas by wet etch processes leaving the metal traces as shown in Figure 4. The wafer is patterned again using photo-sensitive resist, this time to expose the areas to be etched through the silicon wafer to form the structure of the arm. The silicon is dry-etched using a Surface Technology Systems (STS) deep reactive ion etcher (DRIE) creating a nearly vertical etch through the silicon wafer.

A critical parameter for the DRIE etch is to maintain a nearly 90 degree etch angle. Figure 4 depicts a typical etch profile for one of the arms. The etch profile is vertical to within 2 degrees. The yield of for production of over 200 arms is about 90% provided that the etcher is functioning properly. Most of the yield loss is due to breakage in handling during final cleaning activities.

Stepped targets for equation-of-state experiments

Stepped targets are used to determine the equation-of-state of material, its stress-density characteristics, at high pressures under transient conditions by studying the propagation of compression waves through materials with various step heights. Steps of silicon can be used either to study silicon as a single crystal or serve as a mandrel for the deposition of other materials. A top view of a series of steps is shown in Figure 5. The process for making these steps is shown in Figure 6 for shallow steps of less than 15 μm step height. The steps can be photo-lithographically patterned and etched in sequence starting with the deepest step first as shown in the process sequence of Figure 6. Photo-resist spun on the wafer is patterned to expose the area of the substrate corresponding to the deepest step. The silicon is etched using a DRIE process to a depth corresponding to the

difference in step heights between the deepest and next deepest steps. The resist is stripped from the wafer and new resist is spun on the wafer. The new resist is patterned to expose both the deepest step and the area of the next deepest step. The silicon is then etched to a depth corresponding to define the next deepest step. During this etch, the deepest step is also etched. Additional steps can be etched similarly. After etching all the steps, a quick polishing etch (44% KOH/ 5% isopropyl alcohol) can remove any residual defects in the silicon etch at the step transitions resulting from any inadvertent accumulation of resist at these transitions during the patterning process. Steps can be etched to a tolerance of plus/minus 1 micron. These steps can be used to either test the material properties of silicon or the etched silicon can be used as a mandrel to create steps in other materials such as metals or diamond. The steps can be filled with other materials via sputtering, evaporative or chemical vapor deposition processes. The wafer can be polished or machined to planarize the deposited material and the silicon removed using KOH or XeF_2 etchants.

For deeper steps, accumulation of the resist in the deep etched features is too great to result in accurate photo-patterning of the stepped features. For these cases, silicon-dioxide masking layers can be used to define the steps prior to silicon etching. In this case a thin, 200 nm layer of silicon dioxide is grown on the wafer. For a two-step silicon mandrel, the silicon dioxide etch-mask is patterned such it is open in the areas corresponding to the total width of the steps. Resist applied over the silicon dioxide layer is used to mask the opening such that the underlying silicon is only exposed for the area of the deepest step. The deepest step is then etched into the silicon using the DRIE process. The resist is removed and the silicon dioxide layer is used as a etch-mask to prevent etching of the silicon except in the exposed areas. The silicon is etched to create the second deepest step. The silicon dioxide can then be removed using a wet or dry etch. In this process, the photo-resist has only been patterned over relatively flat substrates allowing precise patterning of the etched features.

Graded Density reservoirs

Micro-fabrication techniques can be used to produce graded density reservoirs. Graded density reservoirs are used in material strength experiments to prevent shocking of the material when the laser energy is quickly applied to the target.

One method for producing graded density material is to fabricate an array of pyramids or cones as shown in Figure 7. The void-fraction of material, and thus the density, changes with height from fully dense at the base to zero density at the peaks where the material is fully voided. This material is useful if the relevant experimental length scale is large compared to the peak-to-peak distance between the pyramids. Polymeric pyramidal arrays can be fabricated in a three-step process. In the first step, deep pits are etched in silicon substrates using the DRIE process. The process is de-tuned to result in a pyramidal etch rather than a straight etch. The silicon pits are then etched using an isotropic wet-etchant (HNA etch: hydrofluoric/nitric/acetic acid) to enlarge the pits until they begin to coalesce at the surface of the silicon. In the third step, the etched structures are filled with polymer. The cured polymer structure is released from the mold by

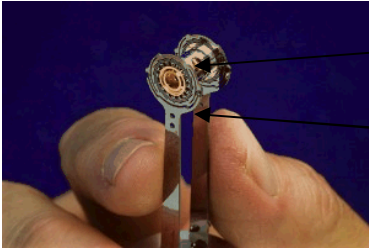
etching away the silicon. Both an epoxy, SU-8, and parylene have been used for the polymer structure. Parylene is more attractive from the fabrication standpoint because the vapor-phase deposition allows deeper molded features to be filled. Parylene results in a poorer shock profile than SU-8, however. Figure depicts arrays of SU-8 pyramids about 8 μm peak-to-peak and about 15 μm high. Pyramids up to about 60 μm tall and 10 μm wide have been produced.

Acknowledgments

This work performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract DE-AC52-07NA27344.

References:

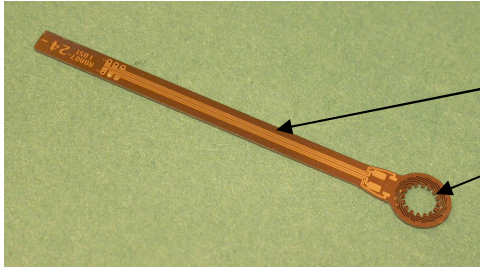
- [1] G. Kovacs, *Micromachined Transducers Sourcebook*, McGraw-Hill, Boston, 1998.
- [2] M. Madou, *Fundamentals of Microfabrication*, CRC Press, 1997.



Target hohlraum

Cooling arms

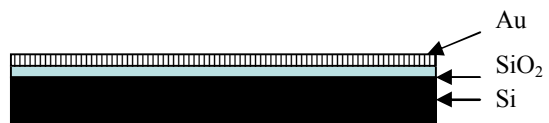
Figure 1. The cooling arms support the target hohlraum in cryogenic experiments
(*courtesy ---*)



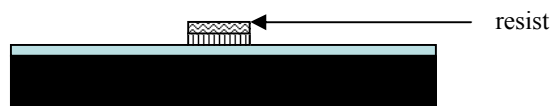
Metal traces

Flexures

Figure 2. Complex flexures can be produced cost-effectively with micro-fabricated parts. Metal traces simplify wiring of the temperature sensor and resistive heaters.



Step 1: Thin film deposition of metal layer



Step 2: Pattern then etch metal traces



Step 3: Pattern then etch silicon parts

Figure 3. Process diagram for micro-fabricated cooling arms to support cryogenic ICF targets

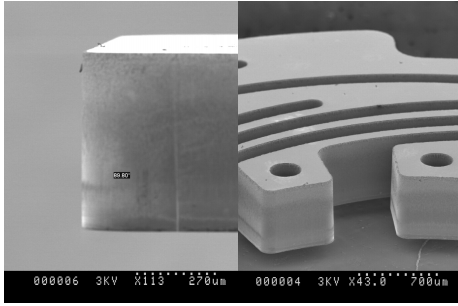
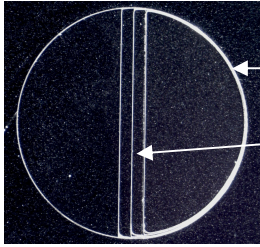


Figure 4. View of DRIE etch of silicon arms showing vertical etch profile



Target perimeter

Step edges

Figure 5. Top view of steps etched in silicon wafer used to test the strength-of-material of silicon or other materials if the silicon is used as a sacrificial mandrel



Step 1: Resist is spun on silicon mandrel



Step 2: The deepest step is etched first



Step 3: Other steps are etched



Step 4: Steps are filled with material to be tested and machined flat



Step 5: Silicon mandrel is removed

Figure 6. Diagram describing method of making stepped structures for strength-of-material tests

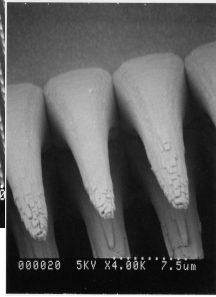
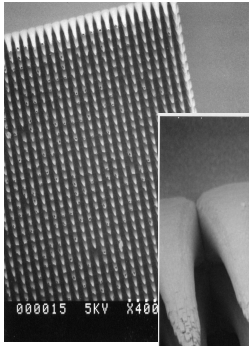


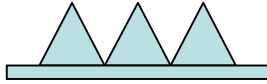
Figure 6. Graded density SU-8 epoxy material exhibiting full density at base and about 5% density at peaks



Step 1: 1 μm wide pyramids are etched in silicon using DRIE



Step 2: The pyramids are opened up using an isotropic wet etch



Step 3: Parylene or SU-8 fills the silicon mold then the silicon is etched away

Figure 8. Process for making pyramidal graded density material